Lab 4 Prelab

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**Lab Partner Name (if you worked together and are submitting the same document or mostly the same answers):**

**Lab Section**: 1

**Submit your prelab document as a PDF file in Canvas under the corresponding prelab assignment. Every student submits their own prelab. Lab partners are allowed to work on the prelab together and submit the same document (if there is actual collaboration on the document). For full credit, the prelab must be submitted prior to the start of lab. Text responses should be typed or printed neatly.**

1. System information

Refer to the following lab resources file: Cybot-Baseboard-LCD-Schematic.pdf. From information given in this file, how might you conclude that serial communication between the CyBot Launchpad board and the PC is using GPIO Port B and UART1?

-PIN mapped test points so one is receiving data inside port b and another pin is transmitting data

1. Port pins for UART1 transmit (TX) and receive (RX)

UART1 is an alternate function, or peripheral, that uses GPIO Port B pins.

1. Which Port B pin is used for the UART1 transmit (TX) signal?
   1. PB1/U1TX/T2CCP1
2. Which Port B pin is used for the UART1 receive (RX) signal?
   1. PB0/URx/T2CCP0
3. Use the GPIO port worksheet below to indicate which Port B pin is used for UART1 TX, which Port B pin is used for UART1 RX, and what values must be initialized in the other GPIO port registers to configure the UART1 alternate function for the port. Put an “x” in cells that you are not using and should preserve their values.

GPIO Port Registers

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Bit >>> vvv Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Description |
| DATA  (or PORT pins for alternate functions) |  |  |  |  |  |  |  |  | 0, 1: bit values  (or alternate functions) |
| DEN | x | x | x | x | x | x | 1 | 1 | 1: enable digital |
| DIR | x | x | x | x | x | x | 0 | 1 | 0: input bit  1: output bit |
| AFSEL | x | x | x | x | x | x | 1 | 1 | 1: enable alternate function |
| PCTL | field | field | field | field | field | field | field | field | Let each column be a 4-bit field in the 32-bit register. |

Refer as needed to mtg08-notes-UART-altfunc.pdf file and Bai book Table 8.1 (in the notes and slides) (see also Tiva datasheet section 23.4 GPIO Pins and Alternate Functions, Table 23-5, for PMCx Bit Field Encoding).

1. Refer to the GPIOAFSEL register description in the Tiva datasheet (Register 10). Refer to the macro definition for the GPIO Port B AFSEL register in the header file, tm4c123gh6pm.h.
2. Write the #define macro definition for the PORTB\_AFSEL register as given in the header file.

#define GPIO\_PORTB\_ASFEL

1. What is the 32-bit memory address of this AFSEL register (in hex)?

0x00000011

1. Explain how to determine this register address from the Tiva datasheet register description (pages 671-672). 0x3 under the PB port line